intermediate semiconductor regions I1-I6, defined between the adjacent pairs of nested insulating regions T2-T8. The first and second semiconductor region R1, R2, and each intermediate semiconductor region I1-I6 are defined in the same semiconductor layer 22. The semiconductor layer 22 in this embodiment is a silicon on insulator layer, but the semiconductor structure may also be formed in bulk silicon, or in some other semiconductor material. In this embodiment each insulating region T1-T8 is a trench isolation structure, but other types of isolation structure may be used.

The voltage isolator 11 further comprises a voltage control device 12. The voltage control device 12 comprises a series of eight Zener diodes D1-D8. Each of Zener diodes D2-D8 is connected in parallel with a corresponding respective insulating region T8-T2. The diodes D1-D8 are connected to each other in series, and each diode D2-D7 has a connection 13 to at least one intermediate semiconductor region I1-I6. Diodes D1 and D2 are both connected to the second semiconductor region R2, and diode D8 is connected to the first semiconductor region R1.

Diode D1 is provided in the second region R2, connected at one end to the semiconductor region R2, and at the other end to a bondpad 33, which is electrically isolated from the semiconductor region R2 by at least one layer of insulating material (such as silicon oxide). Each of diodes D2-D7 is defined in a respective intermediate semiconductor region I6-I1.

Each of the diodes D1-D8 comprises a plurality of sub-diodes, connected in series. In this example, eight sub-diodes are used for each diode (thereby providing a diode with a threshold voltage eight times higher than each sub-diode). The appropriate number of sub-diodes in each diode D1-D8 depends on factors such as the threshold voltage of each diode D1-D8 and the desired maximum voltage across each insulation region 19. The threshold voltage of each sub-diode may be approximately 9.5V, and the threshold voltage of each diode is thereby approximately 76V.

The arrangement of the diodes D1-D8 and the sub-diodes thereof can be seen more clearly in FIG. 8, which shows a detailed view of diode D7 and D8. FIGS. 9 and 10 are sectional views taken along B-B' and A-A' respectively.

Each diode D1-D8 is defined in the silicon on insulator (SOI) layer 22, which is separated from the underlying silicon substrate 21 by a buried oxide layer 20. In this embodiment the buried oxide (BOX) layer is approximately 3 microns thick, and is capable of standing off a voltage of at least 700V. The SOI layer 22 is n type silicon, and is approximately 1.5 microns thick. The invention is equally applicable to p type SOI and to SOI and BOX layers with different thicknesses (as well as to non-silicon semiconductor layers, and to semiconducting layers without a buried insulating layer).

Each sub-diode D71, D78, D81, D88, etc comprises a p doped well (pwell) 23 surrounding a central shallow low ohmic n implanted (n+) region 25. In this embodiment the pwell 23 is square, and the n+ region 25 is octagonal, but other shapes for both the pwell 23 and n+ region 25 may be used as appropriate (e.g. rectangular, oval, circular etc). A p-n junction is thereby formed between the pwell 23 and the n+ region 25. A further annular low ohmic shallow p type implant (p+) region 26 is provided around the n+ region 25 to allow the first metal layer 29 to make ohmic contact with the pwell 23. The pwell 23 is surrounded by a trench isolation 19 to provide lateral voltage isolation of the sub-diode from the surrounding semiconductor layer 22.

The first metal layer 29 connects each sub-diode of each diode D1-D8 in series. For example, referring to diode D8 (shown in FIG. 8), an anode connection 18 of the first sub-diode D81 is connected to the cathode connection 17 of the next sub-diode D82. Similar connections, defined in the first metal layer 29, exist between each of the other sub-diodes. Connections between the first metal layer 29 and each n+ region 25 and p+ region 26 are defined by a first set of conducting vias 27, the layout of which are shown in FIG. 11. These conducting vias 27 can also been seen in FIGS. 9, 10 and 12.

In the final sub-diode D88 of diode D8, the anode connection 18 is also provided with a connection 15 to the first semiconductor region R1, via an n+ region 25 and nwell 24. The final sub-diode of diode D1 is provided with a similar connection 14 to the second semiconductor region R2. Each of diodes D2-D7 has, at its respective final sub-diode, a connection 13 to the intermediate semiconductor region I6-I1 within which the diode D2-D7 is formed. An example of this connection 13 is shown in more detail in FIGS. 11 and 12, in which the contact 13 from sub-diode D78 to the intermediate semiconductor region I1 is shown. Connections 15, 14 to the first and second semiconductor regions R1, R2 are made in the same way.

In the example embodiment of FIGS. 7 to 12, the semiconductor structure 100 is configured to act as a high voltage Zener diode, with a breakdown voltage of 608V (8×8×9.5V). When a voltage of at least of 608V is provided at bondpad 33, and the connection 15 is grounded (for instance via a further bondpad, or by a connection to a further circuit on the same die), the voltage of the second semiconductor region R2 and each intermediate semiconductor region I1-I6 will be fixed at a voltage defined by the breakdown voltage of the diodes D1-D8. I1 will be fixed at 76V, I2 at 152V, I3 at 228V, I4 at 304V, I5 at 380V, I6 at 456V, and I2 at 532V.

In an alternative arrangement, a further Zener diode could be included in the arrangement of FIG. 7, connected in parallel with insulating region T1. With this approach, the region outside the insulating region T1 in FIG. 7 would be the first region, and further voltage step of 76V would be provided between this first region and the second region. The breakdown voltage of the Zener with this extra diode would be 684V. This sort of arrangement is that used in FIG. 13, in which the first region R1 is outside the last insulating region T1, and there is one more Zener diode D1-D6 than there are insulating regions T1-T5.

Although an embodiment has been shown in which the last sub-diode of each diode is connected to the semiconductor region in which the diode is formed, this is not necessarily essential. In some embodiments the first sub-diode (or any other sub-diode) may be connected to the semiconductor region in which the diode is formed.

A semiconductor structure 10 according to the invention can also be configured as a high voltage isolation structure, as shown in FIG. 13. In this arrangement a first semiconductor region R1 is separated from a second high voltage semiconductor region R2 by a voltage isolator 11. The voltage isolator 11 comprises a nested series of insulating regions T1-T5. Intermediate semiconductor regions I1-I4 are defined between each adjacent pair of nested insulating regions T1-T5. A voltage control device 12, comprising a series of Zener diodes D1 to D6 is provided, which controls the voltage across each insulating region T1-T5 when a high bias voltage is placed on the second semiconductor region R2 (relative to the first region R1).

The diodes may be similar to those used in the structure of FIGS. 7-12, comprising eight sub-diodes and having a breakdown voltage of 76V. In this embodiment, the first sub-diode of each diode has a connection 13, 14, 15 to the